

# MAC (Media Access Control) Design and Implementation of DSRC (Dedicated Short Range Communication) Systems

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## Abstract

Dedicated short range communication (DSRC) system is the key technology of intelligent transportation system (ITS), and the associated service information and control commands of ITS can transmit via DSRC. In this paper, we design and implement a DSRC MAC in ARM embedded systems and FPGA chips, including both the DCF and PCF.

## I. Introduction

Intelligent transportation system (ITS) is a very hot research topic in many kinds of fields. This will obviously change the public senses of land transportations, but the architectures are still far from realization, that many key technologies have not be available yet. The main issues of ITS are the transportation management policy and security maintenance, and the information about these need absolutely stable and reliable communication media to transmit. DSRC technologies just play the role. DSRC includes two types of communication model; one is the vehicle to vehicle (v2v) communication, provides the carious sensors' information exchanging and decision and/or control commands transmission between different transportations. The other one is vehicle to roadside (v2r) communication, and this gives the ability to transmit the service information from service center to running vehicles via roadside access points.

Figure 1 shows the proposed ITS architecture, we can clearly find the role of DSRC in the associating applications. And Figure 2 shows the DSRC spectrum allocation in 5.9 GHz permitted by FCC in 1999. There are three types of channels in plan, v2v channel, control channel, and v2r channel. ASTM committee E17.51 has proposed the newest draft version of DSRC in ASTM E2213-03, 2003. The drawn MAC schemes are mostly following the IEEE 802.11 MAC, and the greater part is deal with the physical layer in OSI. Under discussions of proposed literature, we summarize that the MAC schemes utilizing in high mobility and wide coverage applications need to be further modified.

In this paper, we first introduce the IEEE 802.11 MAC roughly, including distributed coordination function (DCF) and point coordination function (PCF). Then, we describe the design and implementation of DSRC MAC prototype. Finally, we give some conclusions and future works of this paper.

## II. IEEE 802.11 MAC Protocol

802.11 was approved by IEEE as an international standard for wireless local area networks (WLAN), including the detail of medium access control (MAC) and physical layer (PHY). The medium access is controlled by the coordination functions, the fundamental DCF and optional PCF in 802.11 standard. We take brief descriptions in the following.

DCF is a random access scheme based on carrier

sense multiple access with collision avoidance (CSMA/CA). Before data transmission, it will detect the channel state in clearance or not. There are two basic principles of DCF transmission: 1).if the channel is idle longer than DCF interframe space (DIFS), the transmission can start, and the carrier sensing could use the physical detection and the network allocation vector (NAV), 2).if the channel is sensed in busy, the transmission should wait until the channel is free, called as access deferral in 802.11, then the exponential backup procedure starts.

PCF adopt the infrastructural access scheme, that only the point coordination unit can manager the medium access. This function is specially implemented in access points (AP), so that the associated stations can only transmit under the admissions of point coordination unit. As the PCF used, the medium will be partitioned into contention-free period (CFP) and contention period (CP), that CFP is coordinated by PCF and CP is DCF. The CFP and CP will exchange in a fixed cycle. As the CFP start, AP will send a beacon frame which includes the CFPMaXDuration field to indicate the time of CFP continuity. All station received the beacon will set their NAV in this value, then DCF stop. When the AP own the medium coordination, it will poll each associated station to send data according to polling list. The CF polling frame is called CF-poll, one CF-poll means the station is licensed to transmit one frame. If the polled station has no response longer than PIFS, AP will assume the polled station has no frame to transmit and poll next station in polling list.

### **III. Design and Implementation**

This section will separate into two subsections, one is the implemented MAC scheme arrangement and the other one is the hardware implementation.

#### **III.1 MAC Schemes**

From the associating literatures and our points of

view, DSRC is inherently not the same to the wireless LAN (WLAN). The conventional WALN is dominated in distributed coordination function (DCF), so that it can realize the carrier sense multiple access with collision avoidance (CSMA/CA) Such MAC scheme is effective in media distribution but not efficiency in utilization rate due to the high overhead. The alternative point coordination function (PCF) in IEEE 802.11 standard is the more efficient scheme than DCF [4]. There are many kinds of mixed frame formats and channel distributions to improve the media utilization rates. So in our plan of DSRC AMC implementations, we use the new type MAC scheme, PCF dominated and DCF assistant, but not the conventional one. We summary the reasons into two terms; one is the application providing that DSRC mainly provide the channel to transmit the ITS service information and control commands, not arbitrary data transmission in WALN. In PCF dominated infrastructure type can guarantee the access of necessary information and commands. The other reason is that, the PCF has more efficient channel utilization to suit the capacity of high mobility.

We arrange the implemented DRSC MAC as a PCF dominated scheme that is based on PCF and assisted with DCF. PCF mainly manager the media access with polling list which included all authenticated and associated stations in the base service set (BSS) coverage. And we open periods of time cyclically in DCF to allow the non-associated and non-authenticated stations to send the management frames and even the v2v transmission. Under the infrastructure architecture, the channel can properly suit the requirements of ITS applications.

#### **III.2 Hardware Implementations**

We utilize the ARM integrator as the hardware platform, shown in Figure 3. ARM integrator mainly includes four modules, that the basic one is Integrator/AP, and it act as a mother-board which has system controller, flash memory, external bus, RS-232, PCI, Compact PCI,

and etc. The second module is core module, CM920T, which can be mounted on the Integrator/AP or used independently. CM920T integrates ARM920T microprocessor, FPGA ASIC (includes SDRAM controller, bus bridge, interrupt controller and etc.), expendable SDRAM (up to 256MB), SSRAM, SSRAM controller, clock generator, Multi-ICE interface, and etc. The third one is logic module, LT-XC2V6000, which mainly has a Xilinx FPGA XC2V6000 on it. The FPGA XC2V6000 has 6M system gates, that's why so called 6000 series. The logic module connectors of LT-XC2V6000 are not in the type of Integrator/AP, so we further need an interface module, IM-LT1, for bridging them. That's the forth module in our hardware platform.

Figure 4 shows the implemented DSRC MAC hardware interface. We use RS-232 serial port to communicate between host PC and ARM development board, so we need to establish the RS-232 decoder to translate the RS-232 information to SSRAM controller compatible ones and to configure the register band. The communications between FPGA and ARM use the AHB bus, and we specify a specific bus to connect the lower MAC and Baseband.

Figure 5 shows the global design architecture of DSRC MAC, it includes the design of driver and upper share memory management (SMM) in host PC, and lower SMM, upper MAC, and lower MAC in network interface card (NIC). We first specify the interface between each segment: 1). between driver and upper SMM, we use the type of function call, that upper SMM provides several interface functions for driver, 2). between upper SMM and lower SMM, we use the type of I/O mapping, that control information is in register band and data transmission is in SSRAM, 3). between lower SMM and upper MAC, we use the type of function call, that lower SMM provides functions for upper MAC, 4). between upper MAC and lower MAC, we use the type of I/O mapping, that use register band in FPGA to transmit

the information to each other, 5). between lower MAC and baseband, we use the register in FPGA to transmit the data and control signals. And the functions of each segment can be described as following:

◆ Diver:

1. Interface between OS and upper SMM.
2. Translation of frame format, between 802.3 and 802.11.
3. Fragment and defragment.
4. Duplication detection and recovery.
5. Unicast and multicast.
6. SME, MAC management service, and MLME.
7. PCF management.

◆ Upper MAC:

1. Set register for lower MAC, including TX queue address, IFS, backoff CW, RTS/CTS flag, RX queue address.
2. Scheduling algorithm.
3. Retry counter.

◆ Lower MAC

1. Set TX rate.
2. Provide the interface to baseband.
3. CCA scheme.
4. Beacon scheme.
5. NAV scheme.
6. FCS generation.
7. Check CRC.
8. Count IFS.
9. Run backoff.
10. Send RTS/CTS.
11. Fill time stamp field.
12. Fill Duration field.
13. Answer ACK.
14. Send data.
15. Set TX rate according to RX rate.

The proposed DSRC MAC includes OS driver design in host PC, ARM microprocessor firmware design, and FPGA circuit design. The integration is successfully

running under RS-232 transmission rate 115Kbs. We design several demonstrations of MAC schemes, and get correct responses in output points with logic analyzer.

#### IV. Conclusions

In this paper, we propose a examine prototype of DSRC MAC. For concerning the DSRC applications and high mobility capacity, we utilize the PCF infrastructure type of MAC to accomplish the role. In the future works, we plan to add some inter access point functions and compact handshaking method to deal with the high mobility issues.

#### Reference

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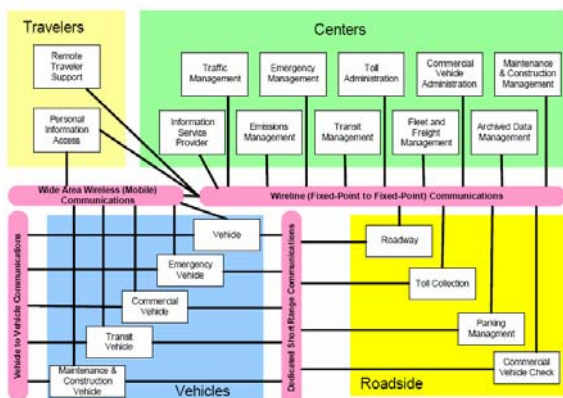


Fig. 1. ITS architecture

(<http://itsarch.iteris.com/itsarch/html/entity/paents.htm>)

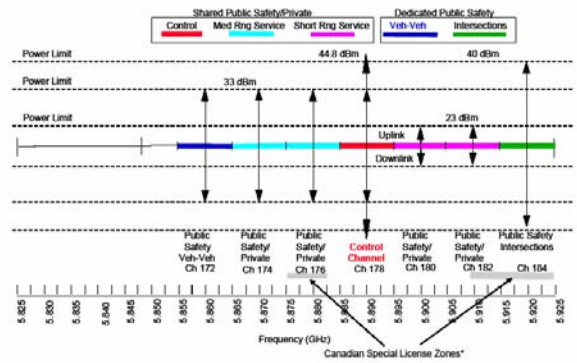


Fig. 2. 5.9GHz DSRC band plan



Fig. 3. Hardware platform

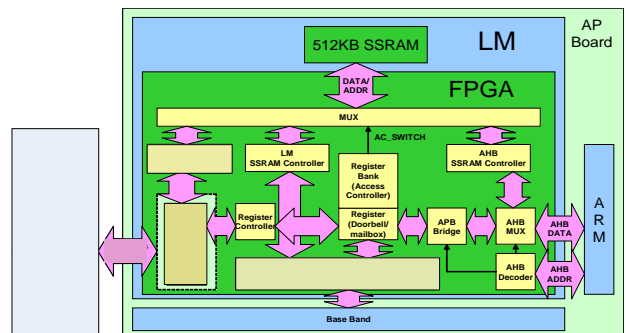


Fig. 4. Diagram of hardware platform

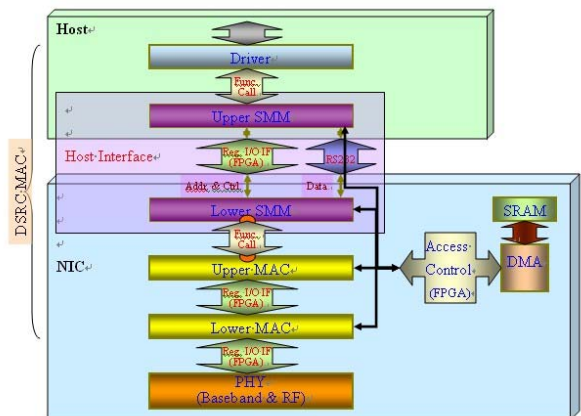


Fig. 5. MAC implementation architecture